Gated SSA

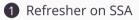
Mechanised Semantics for Gated Static Single Assignment

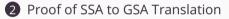
Yann Herklotz² Delphine Demange¹ Sandrine Blazy¹

CAS Seminar, 31 October 2022

¹ IRISA & Inria de l'Université de Rennes

² Imperial College London







3 Summary and On-going Work

Refresher on SSA

Now widely adopted in compiler community

GCC, LLVM, Java HotSpot JIT...

SSA: Variables with unique definition point

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Straight-line code

Definitions: fresh variable, version number Uses: rename variable, pick right version



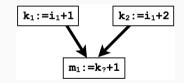
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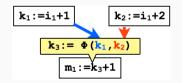
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SSA strengths

CFG-based representation: simple operational semantics ϕ -functions already capture def/use dependencies

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Gated SSA: gates turn control-dep. into data-dep.

Building block of Program Dependence Web [Ottenstein et al., 1990] Ignore some dependencies [Havlak, 1994] Symbolic analysis for parallelizing compiler [Tu and Padua, 1995] Gated SSA: extends ϕ -instructions with gates

Simple join points:

Gates *p_i* discriminate arguments, local choice Pure data-dependency

$$r_d \leftarrow \gamma(\overrightarrow{(p_i, r_i)})$$

Gated SSA: extends ϕ -instructions with gates

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Loop-header join point:

Idea: no adequate gate for iterations Introduce a special node, with built-in looping semantics Analyze loop-carried dependencies $r_d \leftarrow \gamma(\overrightarrow{(p_i, r_i)})$

 $r_d \leftarrow \mu(r_0, r_i)$

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Loop exit point:

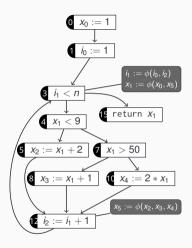
Idea: decouple loop-carried variable from end-of-loop usage Gate p signals when r_s has reached a stable value

$$r_d \leftarrow \gamma(\overrightarrow{(p_i, r_i)})$$

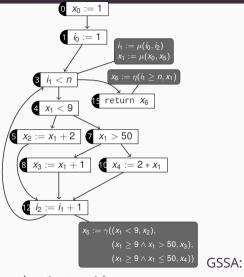
 $r_d \leftarrow \mu(r_0, r_i)$

 $r_d \leftarrow \eta(p, r_s)$

Gated SSA (GSA): example



SSA



extends ϕ -instr. with gates

Gated SSA: State of Affairs

Recent usages

HLS, GPU code gen., parallelizing compilers Non-verified translation validation for LLVM [Tristan et al., 2011] Key component, alas not described in papers!

Numerous variants

Each come with own notion of dependencies No reference implementation, no specification No formal semantics, partial and informal prose

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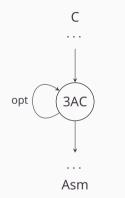
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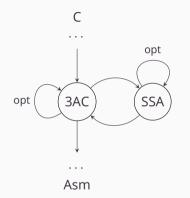
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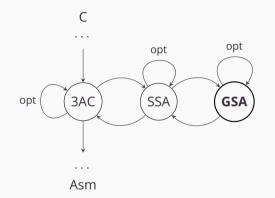
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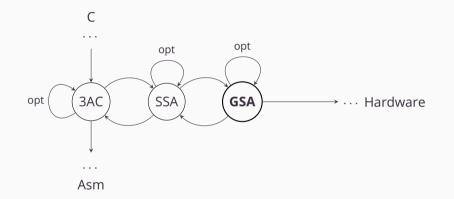
Disclaimer

Necessarily geared to application case Baby steps: focus on gates and generation No performance evaluation yet!









Proof of SSA to GSA Translation

```
Theorem compiler_correct: forall P P' behavior,
    compiler P = OK P' ->
    prog_asm_exec P' behavior ->
    prog_src_exec P behavior.
Proof. [...] Qed.
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Proof. [...] Qed.
```

 Define syntax and semantics for languages: Coq data-structures, Coq relations

- Program the compiler: Coq function
- 3 State the correctness theorem: Coq property
- Prove it, using a simulation diagram: Coq proof script

Single-source path expression problem

"Find, for each vertex v, a regular expression P(s, v) which represents the set of all paths in G from s to v." — [Tarjan, 1981]

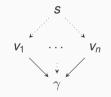
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 μ instructions can be translated directly from ϕ instructions.

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For every future γ node, get a path-expression from the dominator s to each of its predecessors $v_1, v_2, ..., v_n$.



Single-source path expression problem

"Find, for each vertex v, a regular expression P(s, v) which represents the set of all paths in G from s to v." — [Tarjan, 1981]

For every future η node, get a path-expression from the corresponding μ to this node.



Different Ways of Verifying a Compiler Pass

Ideally you want to *fully verify* the translation.

What does that mean?

No proof code should be present at *runtime*.

Why might that not be possible?

Properties might be easy to check but tedious to prove.

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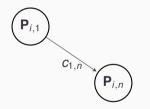
LEMMA 1. Let (P_1, v_1, w_1) , (P_2, v_2, w_2) , ..., (P_i, v_i, w_i) be a path sequence for G and let v be any vertex. After i iterations of the loop in SOLVE, P(s, v) is an unambiguous path expression representing exactly Λ (if s = v) and all nonempty paths p from s to v for which there is a sequence of indices $1 \le i_1 < i_2 < \cdots < i_k \le i$ and a partition of p into $p = p_1, p_2, \ldots, p_k$ such that $p_j \in \sigma(P_{i_j})$ for $1 \le j \le k$.

PROOF. Straightforward by induction on ι .

Instead of proving correctness of *path expressions*, check properties of *predicates*.

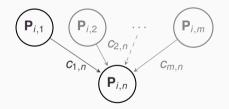
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One core *invariant* we want to maintain is *predicate evaluation*:



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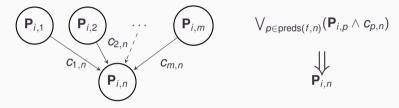
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(Local) Coherence property

f is the SSA function

i and *n* are nodes in CFG of *f*, with *i* strictly dominates *n*

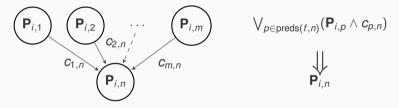


$$f \models \mathbf{P} \operatorname{coh}(i, n)$$

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Evaluability of predicates

Predicates: piece of syntax

Variables in conditions not always defined at runtime: use of a 3-valued logic

 $f \models \mathbf{P} \operatorname{coh}(i, n)$

Intuition

In $r_d \leftarrow \gamma((p_1, r_1), (p_2, r_2))$, p_1 and p_2 must be enough to pick one r_i

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Definition (Mutually exclusive predicates)

 p_1 and p_2 are mutually exclusive, written $p_1 \ltimes p_2$, whenever for all registers state *rs* they cannot both evaluate to true, *i.e.* if $rs \models_p p_1 \Downarrow 1$, then $rs \models_p p_2 \not\Downarrow 1$.

- The properties we are trying to check are arbitrary logic properties.
- The solver needs to use three-valued logic.
- SMT solvers can do all this.

 $\bigvee_{p \in \mathsf{preds}(f,n)} (\mathbf{P}_{i,p} \wedge c_{p,n})$ $\mathbf{P}_{i,n}$

We are not done... The SMT solver would have to be trusted, which does not integrate with our proof.

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SMTCoq¹ is a formalisation of SMT unsatisfiability proofs.

However, their main use case is as:

- 1 a standalone tool, or
- **2** as a Coq tactic to solve Theorems in Coq.

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- **2** as a Coq tactic to solve Theorems in Coq.

We need a checker that can be integrated into the compiler, which will give us the same correctness guarantees.

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The main workflow to prove the SMT solver:

Convert recursive predicates into efficient flat list structure using linear arithmetic to implement three-valued logic:
 P₁ ∧ (P₂ ∨ P₃) into

$$\begin{array}{l} -1 \leq P_1 \leq 1 \land -1 \leq P_2 \leq 1 \land -1 \leq P_3 \leq 1 \land -1 \leq P_4 \leq 1 \land -1 \leq P_5 \leq 1 \\ \land (P_2 < P_3 ? P_4 == P_3 : P_4 == P_2) \\ \land (P_1 < P_4 ? P_5 == P_1 : P_5 == P_4) \\ \land \neg (P_5 == 1) \end{array}$$

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2 Reverse engineer any optimisations that SMTCoq would do on Coq goals.

Prove semantic preservation between initial predicates and SMTCoq formulas.

Many Limitations

• Very slow compilation time due to many SMT checks.

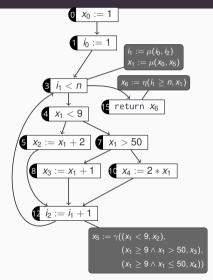
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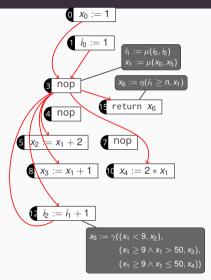
- Very slow compilation time due to many SMT checks.
- Some comparisons are not supported ((unsigned)x == (unsigned)y).
- Destruction of GSA is currently not proven correct.

A Note on GSA to Hardware Conversion



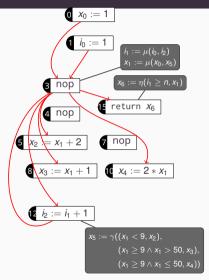
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A Note on GSA to Hardware Conversion



- Currently we only implemented control-flow semantics for GSA.
- One can formulate Dataflow semantics.
- It should map quite nicely to circuits (however efficiency becomes an issue).

Summary and On-going Work

Implementation within CompCertSSA

Prior pass needed for Gated SSA: loop normalization Gated SSA: syntax and semantics Correct generation of Gated SSA

On-going work: destruction of Gated SSA to SSA

• Rebuild control-flow information, conforms to CFG

Future work: 3 Ph.D. projects starting in Rennes and London

Full-fledge gated SSA as a dependency graph Integrate into verified dynamic HLS toolchain

Any Questions?

Semantics of Gated SSA

$$\begin{array}{c|c} \text{Eta} & i = r_d \leftarrow \eta(q, r) & rs \models_p q \Downarrow 1 & b_\eta \vdash rs \stackrel{\mathcal{E}}{\leadsto} rs' \\ \hline i = r_d \leftarrow \eta(q, r) & rs \models_p q \Downarrow 1 & b_\eta \vdash rs \stackrel{\mathcal{E}}{\leadsto} rs' [r_d \mapsto rs(r)] \end{array}$$

$$\begin{array}{c} \text{Merge}_{\gamma} & \text{Merge}_{\mu} \\ i = r_d \leftarrow \gamma(\overrightarrow{(q, r)}) & rs \models_p q_n \Downarrow 1 & i = r_d \leftarrow \mu(r_0, r_1) & k \in \{0, 1\} \\ \hline b_{\mathcal{M}, k \vdash rs \stackrel{\mathcal{M}}{\leadsto} rs'} \\ \hline i :: b_{\mathcal{M}, k \vdash rs \stackrel{\mathcal{M}}{\longleftrightarrow} rs' [r_d \mapsto rs(r_n)] & \overline{i :: b_{\mathcal{M}, k \vdash rs \stackrel{\mathcal{M}}{\leadsto} rs'} rs' [r_d \mapsto rs(r_k)]} \\ \end{array}$$

$$\begin{array}{c} \text{NJoin} & \text{Join} \\ f.\mathcal{I}(l) = \lfloor \text{Inop}(l') \rfloor & f \not\uparrow l' & f.\mathcal{I}(l) = \lfloor \text{Inop}(l') \rfloor & f \lor l' \\ f.\mathcal{E}(l) \vdash rs \stackrel{\mathcal{E}}{\leadsto} rs' & f.\mathcal{M}(l') = \lfloor b_{\mathcal{M}} \rfloor & f.\mathcal{E}(l) \vdash rs \stackrel{\mathcal{E}}{\underset{\tau}{\leadsto} rs'} rs' \\ \hline preds(f, l')_k = l & b_{\mathcal{M}, k \vdash rs' \stackrel{\mathcal{M}}{\longleftarrow} rs'' \\ \vdash \mathcal{S}(f, l, rs) \rightarrow \mathcal{S}(f, l', rs') & \end{array}$$

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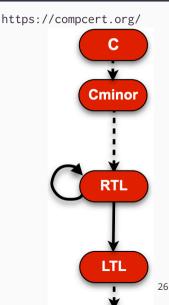
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Verified Compilers: CompCert

X.Leroy, S.Blazy et al. 2005-present

From CompCert C down to Assembly

20 passes, 11 IRs, targets PPC, ARM, x86, Risc-V Optos: const. prop., CSE, DCE, tailcalls, inlining **Formally verified using the Coq proof assistant** Compiler programmed, specified, and proved in Coq Extracted to efficient OCaml code



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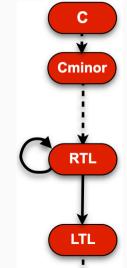
CompCert is mature, commercialized by AbsInt

Airbus (fly-by-wire soft.), MTU (control soft. for emergency power generators)

Conformance to the certification process IEC 60880

Performance gain in estimated WCET

2022: ACM Software System award, ACM SIGPLAN Programming Languages Software award



https://compcert.org/

- Gated SSA, a compiler IR famous for:
 - optimizations in parallelizing compilers [Arenaz et al., 2008]
 - high-level synthesis [Derrien et al., 2020]
 - code generation for GPUs [Sampaio et al., 2012]
- Semantics and correctness of generation
- Focus on gates, in isolation of other challenges

Introduced in late 80's [Alpern et al., 1988]

Now widely adopted in compiler community

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Straight-line code

Definitions: fresh variable, version number Uses: rename variable, pick right version

x := 1	SSA	$x_1 :=$	1
y:= x+2	$\xrightarrow{}$	$y_1 :=$	x 1+2
$\mathbf{x} := \mathbf{y} + \mathbf{x}$		x ₂ :=	$\mathbf{y}_1 + \mathbf{x}_1$

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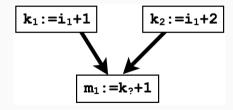
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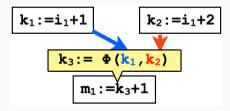
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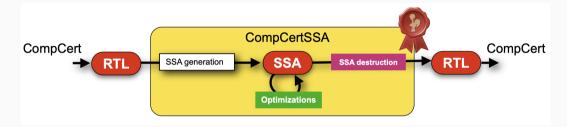
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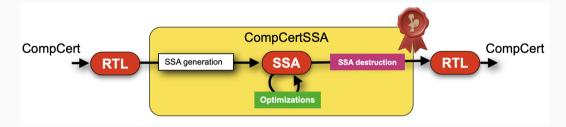
CompCertSSA: an SSA-based Middle-end for CompCert



Middle-end: optimization

RTL: 3-address code, virtual registers, CFG representation SSA: RTL + ϕ -instructions + invariants **Realistic implementation:** GVN, sparse cond. c. pro., coalescing State-of-the-art, similar to LLVM and GCC

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State-of-the-art, similar to LLVM and GCC

Ultimate goals

Understand semantic foundations of SSA techniques Same formal guarantees as CompCert No negative impact on code performance

SSA: semantics

Challenges: integrate well in CompCert compiler chain Be close to RTL semantics Be as intuitive as informal definition given in [Alpern et al., 1988]

Execution states and transition relation, as in RTL

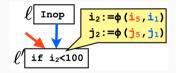
 $\vdash \mathcal{S}(f, I, rs) \rightarrow \mathcal{S}(f, I', rs')$

Execute in a single small-step:

- ① current instruction
- **2** and potential ϕ -block at successor label

Remarks:

Prior RTL normalization: only an Inop can lead to a join point Parallel assignment semantics for ϕ -blocks



SSA strengths

CFG-based representation: simple operational semantics ϕ -functions already capture def/use dependencies

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Numerous variants

Each come with own notion of dependencies No reference implementation, no specification No formal semantics, partial and informal prose

 \Rightarrow We need a semantics and some expected properties for this critical component

Disclaimer

Baby steps: focus on gates and generation No performance evaluation yet! **Predicates**: Main technical point in generation algorithm Generation algorithm: Single-source path expression problem (regexp on path cond.) [Tarjan, 1981]

Predicate matrix P

Gates: syntactical, global information $\mathbf{P}_{i,j}$ = set of paths from *i* to *j* in CFG of *f*

Two intrinsic properties for $r_d \leftarrow \gamma((p_1, r_1), (p_2, r_2))$

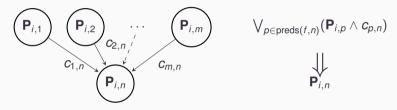
- Coherence: gates are characterizing correct paths
- Well-exclusivity: gates in γ -functions are precise enough **Intuition**: in $r_d \leftarrow \gamma((p_1, r_1), (p_2, r_2), (p_3, r_3))$, p_1, p_2 and p_3 must be enough to pick one r_i

Coherence Property of Predicates

(Local) Coherence property

$$f \models \mathbf{P} \operatorname{coh} (i, n)$$

f is the SSA function *i* and *n* are nodes in CFG of *f*, with *i* strictly dominates *n*



Evaluability of predicates

Predicates: piece of syntax

Variables in conditions not always defined at runtime: use of a 3-valued logic

Implementation within CompCertSSA

Prior pass needed for Gated SSA: loop normalization Gated SSA: syntax and semantics Correct generation of Gated SSA

On-going work: destruction of Gated SSA to SSA

• Rebuild control-flow information, conforms to CFG

Future work: 3 Ph.D. projects starting in Rennes and London

Full-fledge gated SSA as a dependency graph Integrate into verified dynamic HLS toolchain